Figure 1

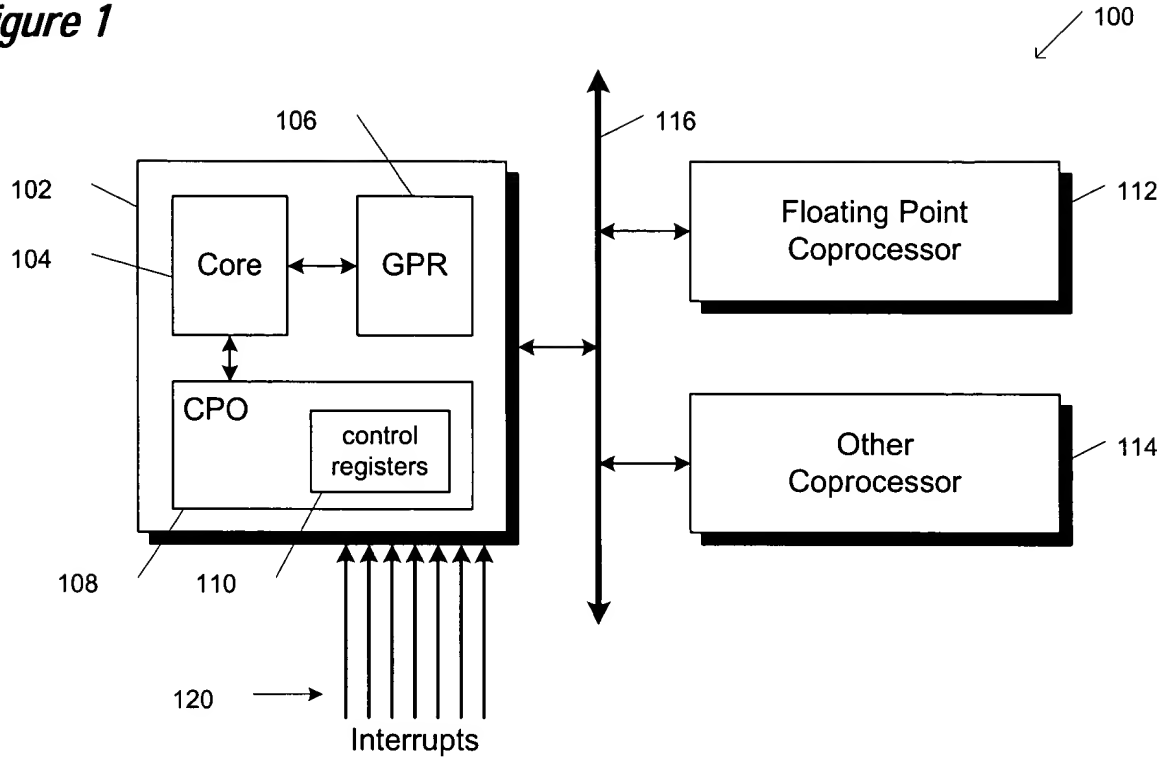


Figure 2

STATUS REGISTER FORMAT

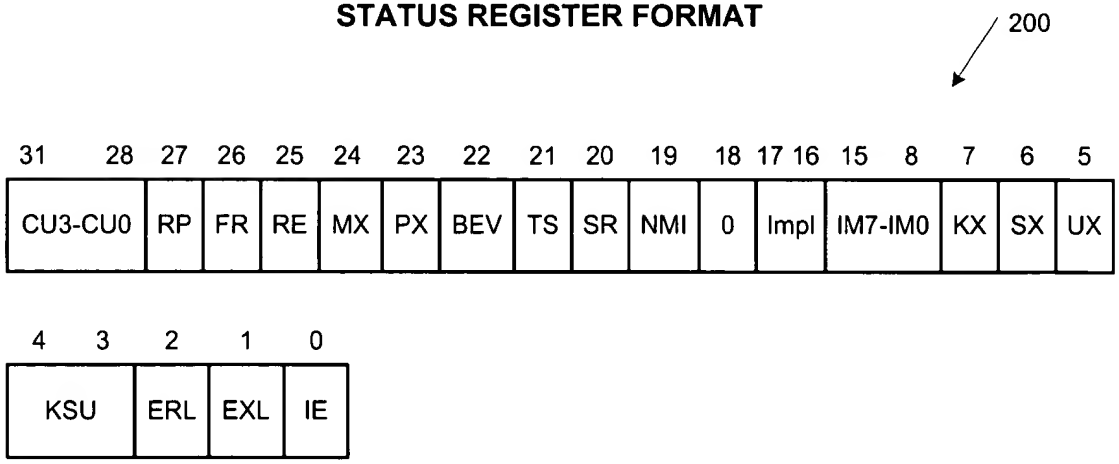


Figure 3

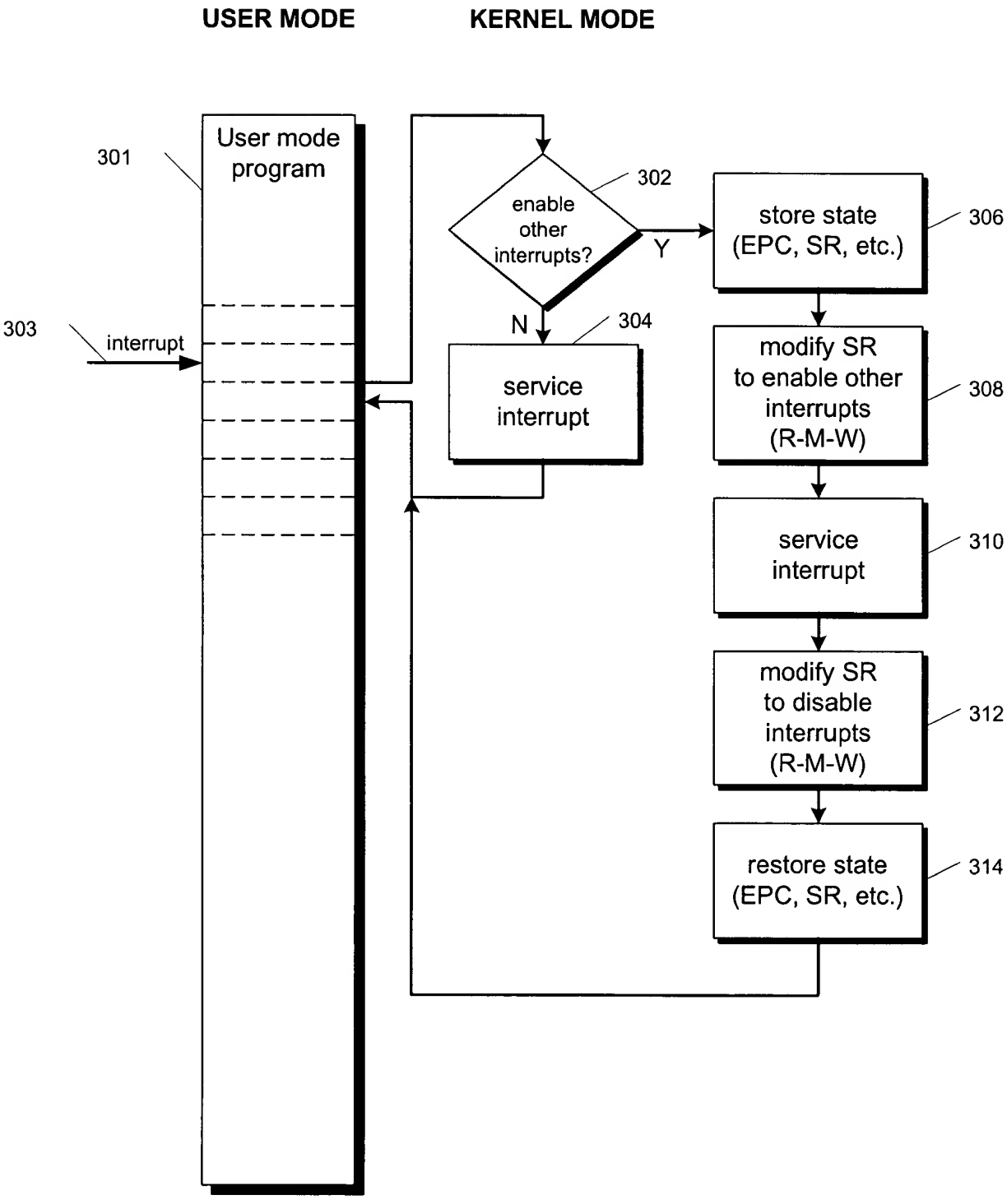

USER MODE
KERNEL MODE
User mode program
301
303
interrupt
enable other interrupts?
302
Y
N
304
service interrupt
store state (EPC, SR, etc.)
306
modify SR to enable other interrupts (R-M-W)
308
service interrupt
310
modify SR to disable interrupts (R-M-W)
312
restore state (EPC, SR, etc.)
314

Figure 4

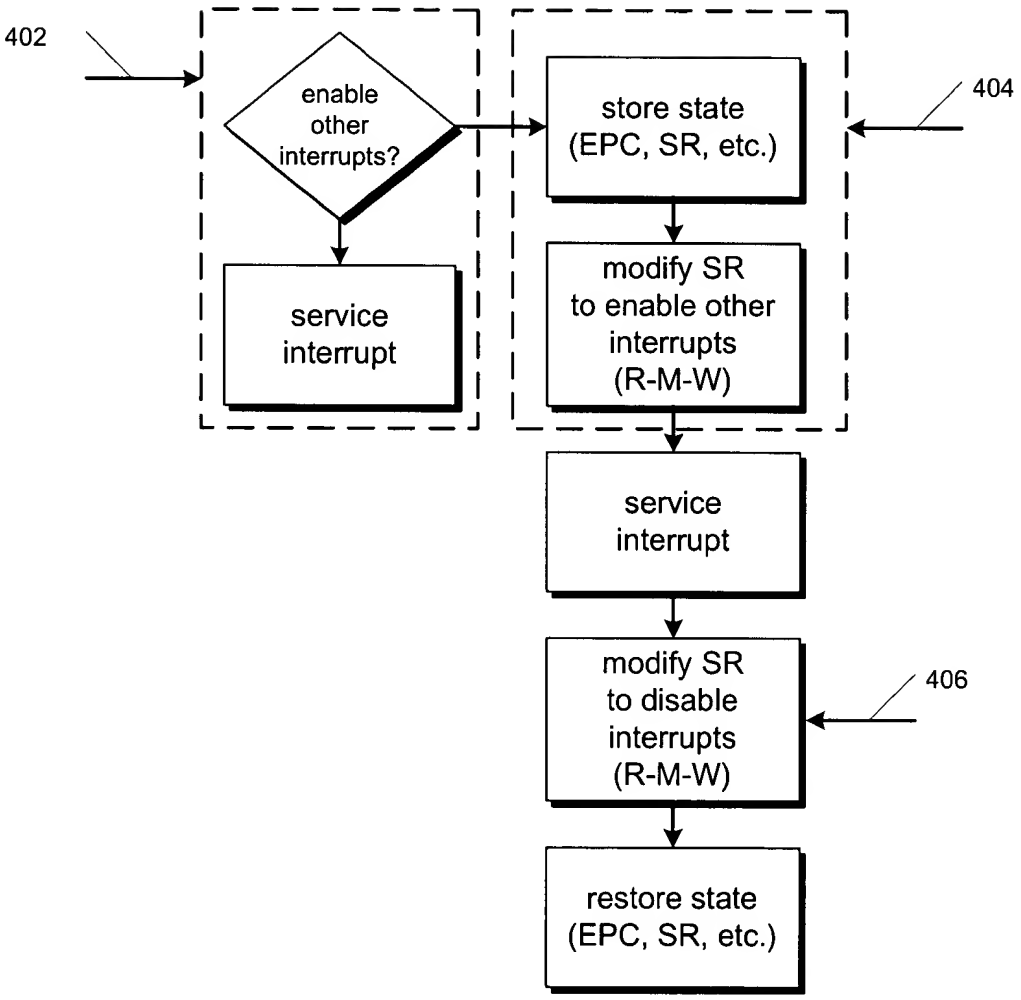

402
enable other interrupts?
service interrupt
store state (EPC, SR, etc.)
404
modify SR to enable other interrupts (R-M-W)
service interrupt
modify SR to disable interrupts (R-M-W)
406
restore state (EPC, SR, etc.)

Figure 5

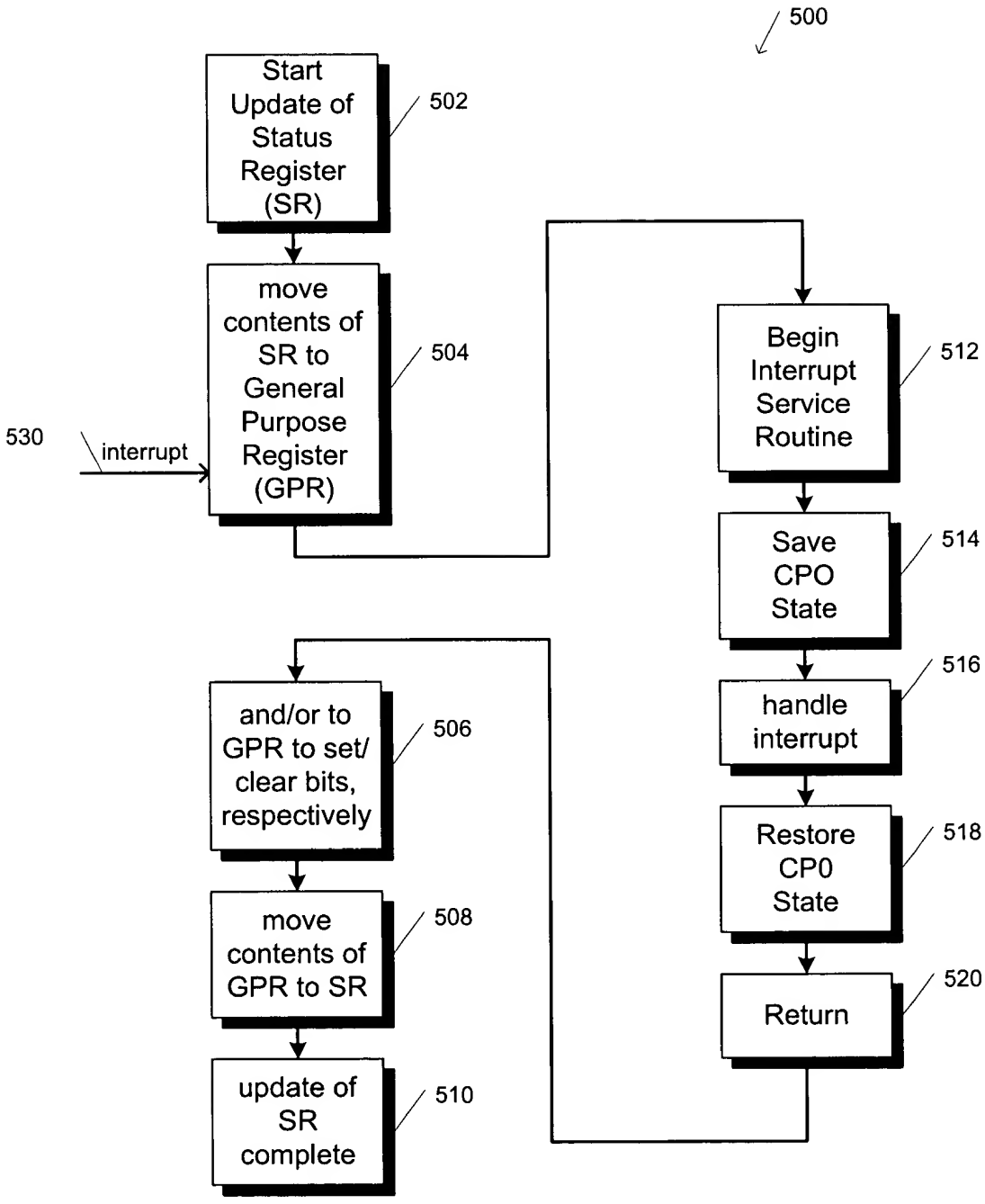
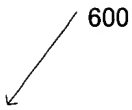

500
Start Update of Status Register (SR)
502
move contents of SR to General Purpose Register (GPR)
504
530
interrupt
and/or to GPR to set/ clear bits, respectively
506
move contents of GPR to SR
508
update of SR complete
510
Begin Interrupt Service Routine
512
Save CPO State
514
handle interrupt
516
Restore CP0 State
518
Return
520

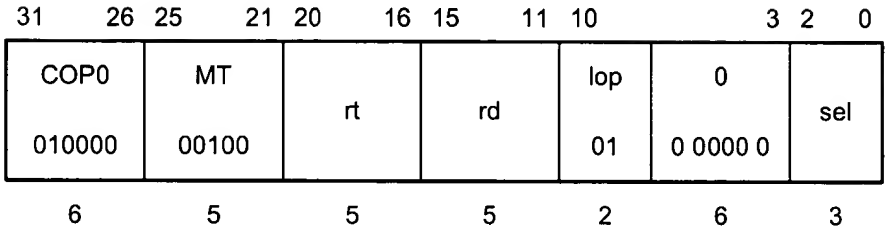
Figure 6



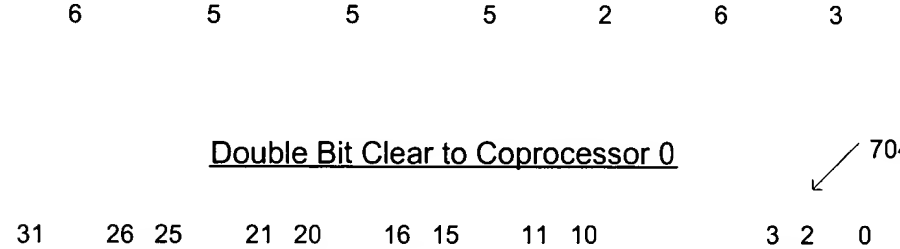
Mnemonic	Function
BICC0	Bit Clear Coprocessor Zero
BISC0	Bit Set Coprocessor Zero
DBICC0	Doubleword Bit Clear Coprocessor Zero
DBISC0	Doubleword Bit Set Coprocessor Zero

Figure 7

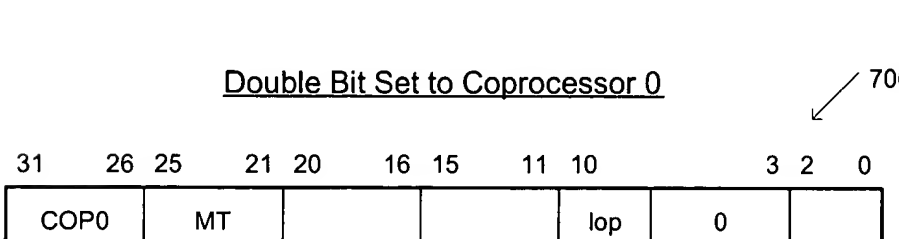
Bit Clear to Coprocessor 0 — 700



Bit Set to Coprocessor 0 — 702

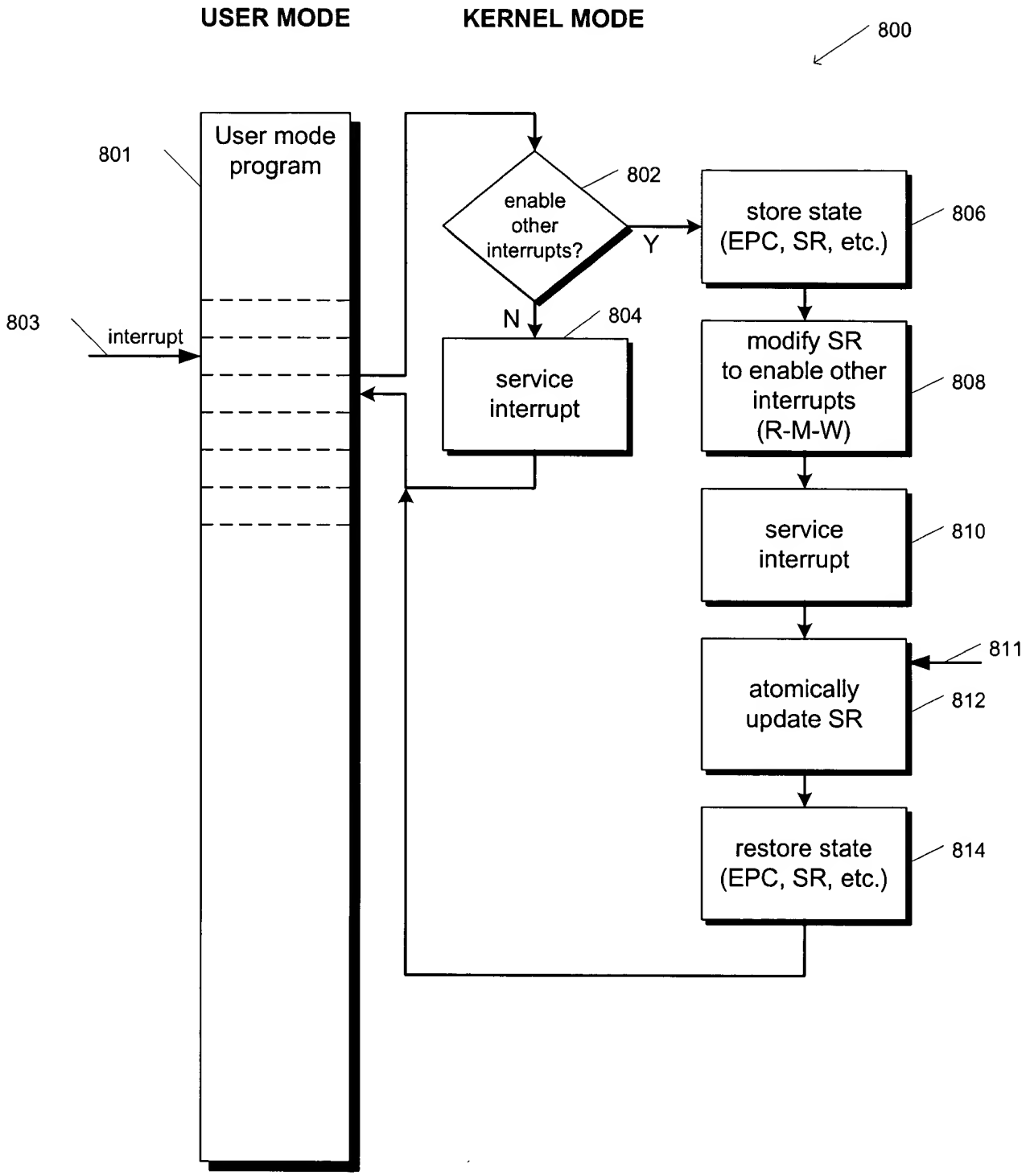


Double Bit Clear to Coprocessor 0 — 704



Double Bit Set to Coprocessor 0 — 706

Figure 8


USER MODE
KERNEL MODE
800
User mode program
801
802
enable other interrupts?
Y
N
store state (EPC, SR, etc.)
806
804
service interrupt
803
interrupt
modify SR to enable other interrupts (R-M-W)
808
service interrupt
810
811
atomically update SR
812
restore state (EPC, SR, etc.)
814